

What Is Claimed Is:

1 1. An arrangement of differential pairs of wires that carry differential
2 signals across a semiconductor chip, comprising:

3 a set of parallel tracks on the semiconductor chip that are used to route the
4 differential pairs of wires;

5 wherein each differential pair of wires includes a true wire and a
6 complement wire that carry corresponding true and complement signals;

7 wherein the differential pairs of wires are non-adjacent, so that each true
8 wire is separated from its corresponding complement wire by at least one
9 intervening wire in the set of parallel tracks, thereby reducing coupling
10 capacitance between corresponding true and complement wires; and

11 one or more twisting structures, wherein a twisting structure twists a
12 differential pair of wires so that the corresponding true and complement wires are
13 interchanged within the set of parallel tracks.

1 2. The arrangement of claim 1, wherein the one or more twisting
2 structures are arranged so that substantially zero net differential coupling
3 capacitance exists for each differential pair of wires.

1 3. The arrangement of claim 2,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 four adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track;

5 wherein the differential pairs of wires include a first differential pair, *A*
6 and \bar{A} , and a second differential pair, *B* and \bar{B} ;

7 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
8 the third track and \bar{B} starts in the fourth track;

9 wherein a first twisting structure causes *B* and \bar{B} to interchange, so that *A*
10 is in the first track, \bar{B} is in the second track, \bar{A} is in the third track and *B* is in the
11 fourth track;

12 wherein a second twisting structure causes *A* and \bar{A} to interchange, so
13 that \bar{A} is in the first track, \bar{B} is in the second track, *A* is in the third track and *B* is
14 in the fourth track; and

15 wherein a third twisting structure causes \bar{B} and *B* to interchange, so that
16 \bar{A} is in the first track, *B* is in the second track, *A* is in the third track and \bar{B} is in
17 the fourth track.

1 4. The arrangement of claim 3,

2 wherein the first twisting structure is located approximately one quarter of
3 the way down the set of parallel tracks;

4 wherein the second twisting structure is located approximately one half of
5 the way down the set of parallel tracks; and

6 wherein the third twisting structure is located approximately three quarters
7 of the way down the set of parallel tracks.

1 5. The arrangement of claim 3,

2 wherein the first twisting structure is located more than one quarter of the
3 way down the set of parallel tracks;

4 wherein the second twisting structure is located more than one half of the
5 way down the set of parallel tracks; and

6 wherein the third twisting structure is located more than three quarters of
7 the way down the set of parallel tracks.

1 6. The arrangement of claim 2,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 four adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track;
5 wherein the differential pairs of wires include a first differential pair, *A*
6 and \bar{A} , and a second differential pair, *B* and \bar{B} ;

7 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
8 the third track and \bar{B} starts in the fourth track; and

9 wherein a first twisting structure causes *A* and \bar{A} to interchange, so that
10 \bar{A} is in the first track, *B* is in the second track, *A* is in the third track and \bar{B} is in
11 the fourth track.

1 7. The arrangement of claim 6, wherein the first twisting structure is
2 located approximately one half of the way down the set of parallel tracks.

1 8. The arrangement of claim 6, wherein the first twisting structure is
2 located more than one half of the way down the set of parallel tracks.

1 9. The arrangement of claim 2,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 six adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track, which is
5 adjacent to a fifth track, which is adjacent to a sixth track;

6 wherein the differential pairs of wires include a first differential pair, *A*
7 and \bar{A} , a second differential pair, *B* and \bar{B} , and a third differential pair, *C* and
8 \bar{C} ;

9 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
10 the third track, *C* starts in the fourth track, \bar{B} starts in the fifth track and \bar{C} starts
11 in the sixth track; and

12 wherein a first twisting structure causes *A* and \bar{A} to interchange, so that
13 \bar{A} is in the first track, *B* is in the second track, *A* is in the third track, *C* is in the
14 fourth track, \bar{B} is in the fifth track and \bar{C} is in the sixth track.

1 10. The arrangement of claim 9, wherein the first twisting structure is
2 located approximately one half of the way down the set of parallel tracks.

1 11. The arrangement of claim 9, wherein the first twisting structure is
2 located more than one half of the way down the set of parallel tracks.

1 12. The arrangement of claim 1,
2 wherein the set of parallel tracks are located within the same metal layer in
3 the semiconductor chip; and
4 wherein the one or more twisting structures use at least one other metal
5 layer to interchange signals between tracks.

1 13. A method for arranging differential pairs of wires to carry
2 differential signals across a semiconductor chip, wherein each differential pair of
3 wires includes a true wire and a complement wire that carry corresponding true
4 and complement signals, the method comprising:

5 defining a set of parallel tracks on the semiconductor chip, which are used
6 to route the differential pairs of wires;

7 mapping differential pairs of wires to tracks so that the differential pairs of
8 wires are non-adjacent, which means that each true wire is separated from its
9 corresponding complement wire by at least one intervening wire in the set of
10 parallel tracks, thereby reducing coupling capacitance between corresponding true
11 and complement wires; and

12 locating one or more twisting structures, wherein a twisting structure
13 twists a differential pair of wires so that the corresponding true and complement
14 wires are interchanged within the set of parallel tracks.

1 14. The method of claim 13, wherein the one or more twisting
2 structures are located so that substantially zero net differential coupling
3 capacitance exists for each differential pair of wires.

1 15. The method of claim 14,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 four adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track;

5 wherein the differential pairs of wires include a first differential pair, *A*
6 and \bar{A} , and a second differential pair, *B* and \bar{B} ;

7 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
8 the third track and \bar{B} starts in the fourth track;

9 wherein a first twisting structure causes *B* and \bar{B} to interchange, so that *A*
10 is in the first track, \bar{B} is in the second track, \bar{A} is in the third track and *B* is in the
11 fourth track;

12 wherein a second twisting structure causes A and \bar{A} to interchange, so
13 that \bar{A} is in the first track, \bar{B} is in the second track, A is in the third track and B is
14 in the fourth track; and

15 wherein a third twisting structure causes \bar{B} and B to interchange, so that
16 \bar{A} is in the first track, B is in the second track, A is in the third track and \bar{B} is in
17 the fourth track.

1 16. The method of claim 14,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 four adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track;
5 wherein the differential pairs of wires include a first differential pair, A
6 and \bar{A} , and a second differential pair, B and \bar{B} ;

7 wherein A starts in the first track, B starts in the second track, \bar{A} starts in
8 the third track and \bar{B} starts in the fourth track; and

9 wherein a first twisting structure causes A and \bar{A} to interchange, so that
10 \bar{A} is in the first track, B is in the second track, A is in the third track and \bar{B} is in
11 the fourth track.

1 17. The method of claim 14,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 six adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track, which is
5 adjacent to a fifth track, which is adjacent to a sixth track;

6 wherein the differential pairs of wires include a first differential pair, *A*
7 and \bar{A} , a second differential pair, *B* and \bar{B} , and a third differential pair, *C* and
8 \bar{C} ;

9 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
10 the third track, *C* starts in the fourth track, \bar{B} starts in the fifth track and \bar{C} starts
11 in the sixth track; and

12 wherein a first twisting structure causes *A* and \bar{A} to interchange, so that
13 \bar{A} is in the first track, *B* is in the second track, *A* is in the third track, *C* is in the
14 fourth track, \bar{B} is in the fifth track and \bar{C} is in the sixth track.

1 18. An arrangement of differential pairs of wires that carry differential
2 signals across a semiconductor chip, comprising:

3 a set of parallel tracks on the semiconductor chip that are used to route the
4 differential pairs of wires;

5 wherein each differential pair of wires includes a true wire and a
6 complement wire that carry corresponding true and complement signals;

7 wherein the differential pairs of wires are non-adjacent, so that each true
8 wire is separated from its corresponding complement wire by at least one
9 intervening wire in the set of parallel tracks, thereby reducing coupling
10 capacitance between corresponding true and complement wires; and

11 one or more twisting structures, wherein a twisting structure twists a
12 differential pair of wires so that the corresponding true and complement wires are
13 interchanged within the set of parallel tracks, and wherein the one or more
14 twisting structures are arranged so that substantially zero net differential coupling
15 capacitance exists for each differential pair of wires;

16 wherein the set of parallel tracks includes a possibly repeating pattern of
17 four adjacent tracks, including a first track, which is adjacent to a second track,
18 which is adjacent to a third track, which is adjacent to a fourth track;

19 wherein the differential pairs of wires include a first differential pair, *A*
20 and \bar{A} , and a second differential pair, *B* and \bar{B} ;

21 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
22 the third track and \bar{B} starts in the fourth track;

23 wherein a first twisting structure causes *B* and \bar{B} to interchange, so that *A*
24 is in the first track, \bar{B} is in the second track, \bar{A} is in the third track and *B* is in the
25 fourth track;

26 wherein a second twisting structure causes *A* and \bar{A} to interchange, so
27 that \bar{A} is in the first track, \bar{B} is in the second track, *A* is in the third track and *B* is
28 in the fourth track; and

29 wherein a third twisting structure causes \bar{B} and *B* to interchange, so that
30 \bar{A} is in the first track, *B* is in the second track, *A* is in the third track and \bar{B} is in
31 the fourth track.

1 19. An arrangement of differential pairs of wires that carry differential
2 signals across a semiconductor chip, comprising:

3 a set of parallel tracks on the semiconductor chip that are used to route the
4 differential pairs of wires;

5 wherein each differential pair of wires includes a true wire and a
6 complement wire that carry corresponding true and complement signals;

7 wherein the differential pairs of wires are non-adjacent, so that each true
8 wire is separated from its corresponding complement wire by at least one

9 intervening wire in the set of parallel tracks, thereby reducing coupling
10 capacitance between corresponding true and complement wires; and
11 one or more twisting structures, wherein a twisting structure twists a
12 differential pair of wires so that the corresponding true and complement wires are
13 interchanged within the set of parallel tracks, and wherein the one or more
14 twisting structures are arranged so that substantially zero net differential coupling
15 capacitance exists for each differential pair of wires;
16 wherein the set of parallel tracks includes a possibly repeating pattern of
17 four adjacent tracks, including a first track, which is adjacent to a second track,
18 which is adjacent to a third track, which is adjacent to a fourth track;
19 wherein the differential pairs of wires include a first differential pair, A
20 and \bar{A} , and a second differential pair, B and \bar{B} ;
21 wherein A starts in the first track, B starts in the second track, \bar{A} starts in
22 the third track and \bar{B} starts in the fourth track; and
23 wherein a first twisting structure causes A and \bar{A} to interchange, so that
24 \bar{A} is in the first track, B is in the second track, A is in the third track and \bar{B} is in
25 the fourth track.

1 20. An arrangement of differential pairs of wires that carry differential
2 signals across a semiconductor chip, comprising:
3 a set of parallel tracks on the semiconductor chip that are used to route the
4 differential pairs of wires;
5 wherein each differential pair of wires includes a true wire and a
6 complement wire that carry corresponding true and complement signals;
7 wherein the differential pairs of wires are non-adjacent, so that each true
8 wire is separated from its corresponding complement wire by at least one

9 intervening wire in the set of parallel tracks, thereby reducing coupling
10 capacitance between corresponding true and complement wires; and
11 one or more twisting structures, wherein a twisting structure twists a
12 differential pair of wires so that the corresponding true and complement wires are
13 interchanged within the set of parallel tracks, and wherein the one or more
14 twisting structures are arranged so that substantially zero net differential coupling
15 capacitance exists for each differential pair of wires;
16 wherein the set of parallel tracks includes a possibly repeating pattern of
17 six adjacent tracks, including a first track, which is adjacent to a second track,
18 which is adjacent to a third track, which is adjacent to a fourth track, which is
19 adjacent to a fifth track, which is adjacent to a sixth track;
20 wherein the differential pairs of wires include a first differential pair, *A*
21 and \bar{A} , a second differential pair, *B* and \bar{B} , and a third differential pair, *C* and
22 \bar{C} ;
23 wherein *A* starts in the first track, *B* starts in the second track, \bar{A} starts in
24 the third track, *C* starts in the fourth track, \bar{B} starts in the fifth track and \bar{C} starts
25 in the sixth track; and
26 wherein a first twisting structure causes *A* and \bar{A} to interchange, so that
27 \bar{A} is in the first track, *B* is in the second track, *A* is in the third track, *C* is in the
28 fourth track, \bar{B} is in the fifth track and \bar{C} is in the sixth track.

1 21. An arrangement of differential pairs of wires that carry differential
2 signals across a semiconductor chip, comprising:
3 a set of parallel tracks on the semiconductor chip that are used to route the
4 differential pairs of wires;

5 wherein each differential pair of wires includes a true wire and a
6 complement wire that carry corresponding true and complement signals; and
7 wherein the differential pairs of wires are non-adjacent, so that each true
8 wire is separated from its corresponding complement wire by at least one
9 intervening wire in the set of parallel tracks, thereby reducing coupling
10 capacitance between corresponding true and complement wires.

1 22. The arrangement of differential pairs of wires of claim 21,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 four adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track;
5 wherein the differential pairs of wires include a first differential pair, *A*
6 and \bar{A} , and a second differential pair, *B* and \bar{B} ; and
7 wherein *A* resides in the first track, *B* resides in the second track,
8 \bar{A} resides in the third track and \bar{B} resides in the fourth track.

1 23. A method for arranging differential pairs of wires to carry
2 differential signals across a semiconductor chip, wherein each differential pair of
3 wires includes a true wire and a complement wire that carry corresponding true
4 and complement signals, the method comprising:

5 defining a set of parallel tracks on the semiconductor chip, which are used
6 to route the differential pairs of wires; and
7 mapping differential pairs of wires to tracks so that the differential pairs of
8 wires are non-adjacent, which means that each true wire is separated from its
9 corresponding complement wire by at least one intervening wire in the set of
10 parallel tracks, thereby reducing coupling capacitance between corresponding true
11 and complement wires.

1 24. The method of claim 23,
2 wherein the set of parallel tracks includes a possibly repeating pattern of
3 four adjacent tracks, including a first track, which is adjacent to a second track,
4 which is adjacent to a third track, which is adjacent to a fourth track;
5 wherein the differential pairs of wires include a first differential pair, *A*
6 and \bar{A} , and a second differential pair, *B* and \bar{B} ; and
7 wherein *A* resides in the first track, *B* resides in the second track,
8 \bar{A} resides in the third track and \bar{B} resides in the fourth track.